

Quantum-dot Cellular Automata Design Guideline

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Abstract – *Quantum-dot Cellular Automata (QCA) can be considered as a candidate for the next generation digital logic implementation technology due to their small feature sizes and ultra low power consumption. Up to now, several designs using QCA technology have been proposed. However, we found not all of the designs function properly. Furthermore, no general design guidelines have been proposed so far. This makes designing a large scale circuits using QCA technology an extremely time-consuming process. In this paper, we show several critical vulnerabilities related to unbalanced input paths to QCA gates and sneak noise paths in QCA interconnect structures. In order to make up the vulnerabilities, a disciplinary guideline will be proposed.*

Keywords: Quantum-dot Cellular Automata, Unbalanced Input Path, Sneak Noise Path, Disciplinary Guideline

1 Introduction

Scaling of CMOS devices is being aggressively pursued by shrinking transistor dimensions, reducing power supply voltages and increasing operating frequencies. Such aggressive scaling adversely results in a series of non-ideal behaviors such as high leakage current and high power density levels. These issues will eventually become road blocks and slow down the scaling trend that exists for years. Quantum-dot Cellular Automata (QCA) is attracting a lot of attention due to their extremely small feature sizes and ultra low power consumption [1].

2 Vulnerabilities in QCA Designs

A crossover is shown in Figure 1(a). However, the simulation [3] result shows that the signal input at cell C fails being transferred to cell Z. The information carried by cell Z is actually the inversion of input at cell A.

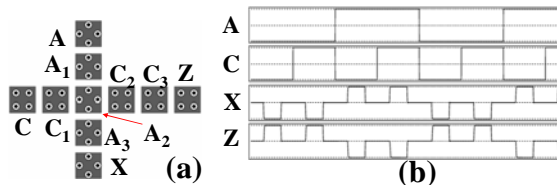


Figure 1 : (a) An extended crossover (b) Simulation result

The effect that the state of one cell has on that of its neighbors can be quantified by a cell-cell response func-

tion. The nonlinearity and bistable saturation of the cell-cell response serves the same role as gain in a conventional digital circuit [4]. A very slight polarization of a cell induces a much larger polarization of its neighbor. The neighbor also feedbacks a larger polarization to the cell even before the neighbor's polarization is saturated. Such synergic effect amplifies not only the polarization of a signal, but also that of a noise.

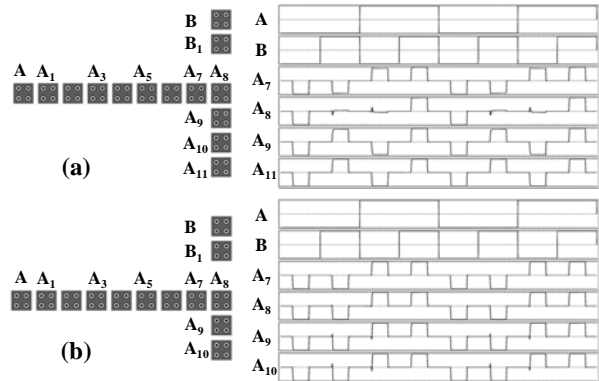


Figure 2 : The noise amplification

In Figure 2(a), two inputs are applied at A and B. From the designer's point of view, the input from A acts as signal while the input from B acts as noise. Although A₇ is closer to A₈ than B₁, the noise from B arrives at A₈ earlier than the signal due to its shorter propagation path, and then propagates down to A₁₀ and A₁₁. The positive polarization feedback between these cells amplifies the noise so that the signal is stuck at A₈, and propagates no further. However, if A₁₁ is removed, the noise-induced polarization is not fully amplified, and the noise disappears as shown in Figure 2(b). This experiment shows that the noise amplification is successful when noises arrive earlier than signals, and the wire segment at the noise injection point is long enough. Therefore, it can be prevented by either limiting this length or letting signal arrive first.

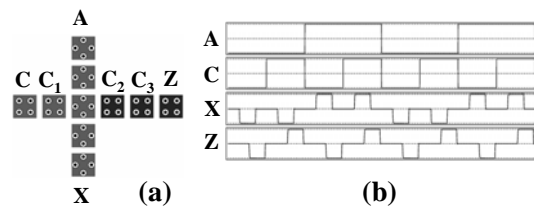


Figure 3 : A working crossover and the simulation result

To prevent the noise amplification on cells C_2 , C_3 and Z in Figure 1, the signal has to arrive at cell C_2 , C_3 and Z no later than noise. This requires a clocked QCA design. The revised crossover and the simulation result are shown in Figure 3. The horizontal wire is segmented into two phases with a 90-degree phase delay in between. The QCA pipeline clocks are represented by different gray levels. During the hold phase of cells C and C_1 , the polarizations of cells C_2 , C_3 and Z are determined simultaneously by signal from C and noise from A and are eventually settle down to signal. The simulation result confirms that the signal on cell C has been successfully transferred to cell Z.

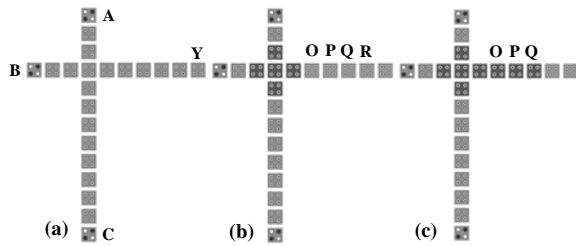


Figure 4 : Majority gates with (a) all cells in a phase (b) a proper clock assignment (c) noise amplification due to an improper clock assignment

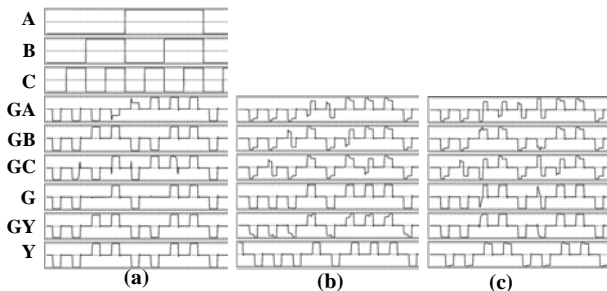


Figure 5 : Simulation results of the majority gates

Consider a majority gate implementation shown in Figure 4(a). Cells A, B and C serve as the inputs and cell Y is the output. All the cells are in a single phase. The simulation, however, shows that this gate does not work as a majority gate as shown in Figure 5(a). Due to the unbalanced input paths, signal from A and B arrive at gate device G earlier than signal from C. The gate device will gain its polarization from cells GA and GB, and then propagate the polarization down to C. Signal from C will lose its chance of voting at gate device G and eventually be stuck at somewhere between GC and C. A functional QCA majority gate with a proper clock assignment and its simulation are shown in Figure 4(b) and Figure 5(b), respectively. Cells GA, GB, GC, GY and G are in a new phase with a 90-degree phase delay than cells A, B and C. Cells GA, GB and GC will gain their polarizations and vote on gate device G at the same time, no matter how unbalanced the three input paths are. However, if cells O, P, Q have the same phase with cells GA, GB, GC and GY as shown in Figure 4(c), faults occur when the signals on cells A and C are all -1 at the third clock cycle, and all 1 at the sixth clock cycle as shown in Figure 5(c). At the third clock cycle, cells GA and GC are temporarily polarized to -1.

Since the placement between cells GA, GC and GY works like an inverter, this in turn polarizes cell GY to 1. Due to the synergic effect of the cell-cell response between cells GY, O, P and Q, this noise is successfully amplified, and cell GY casts a vote for 1 at the majority gate. The fault at the sixth clock cycle can be similarly explained.

3 ALU Case Study

Towards validating the proposed disciplinary rules for robust QCA designs, we redesigned the bit slice of the Simple 12 ALU which was presented in [2]. The original design was not operational mostly due to the sneak noise path in the crossover structure, and the asynchronous signal flow of the gate structure. The QCA pipeline clocks are assigned to the cells so that the noise in crossovers can be tolerated, and the signal flows in gates can be synchronized. This bit slice of the Simple 12 ALU is implemented in the area of 58×81 grids² using 1030 cells, and operates at a clock rate of 1 THz. The latency of a 1-bit operation is 34 clock phases (8.5 clock cycles). The functional correctness has been verified by simulation although the results are not shown here due to the limited space.

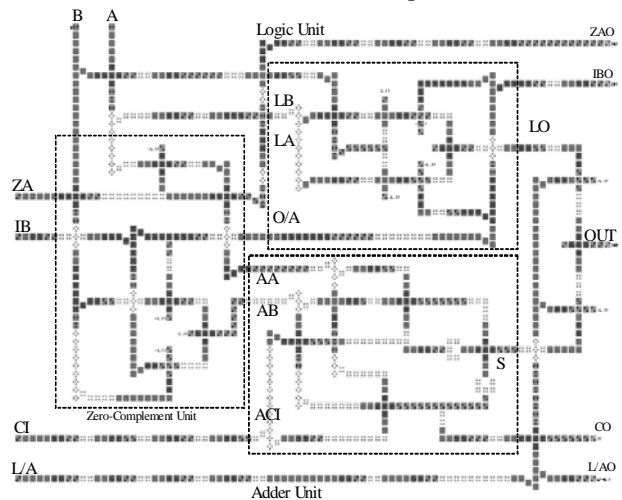


Figure 6 : Schematic of the Simple 12 ALU bit slice

4 Conclusions

Most of QCA designs from previous work cannot function properly. In this paper we have identified several primitive design patterns that will fail due to noises of multiple inputs. A set of disciplinary rules that can effectively suppress noises is presented for robust QCA designs.

References

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